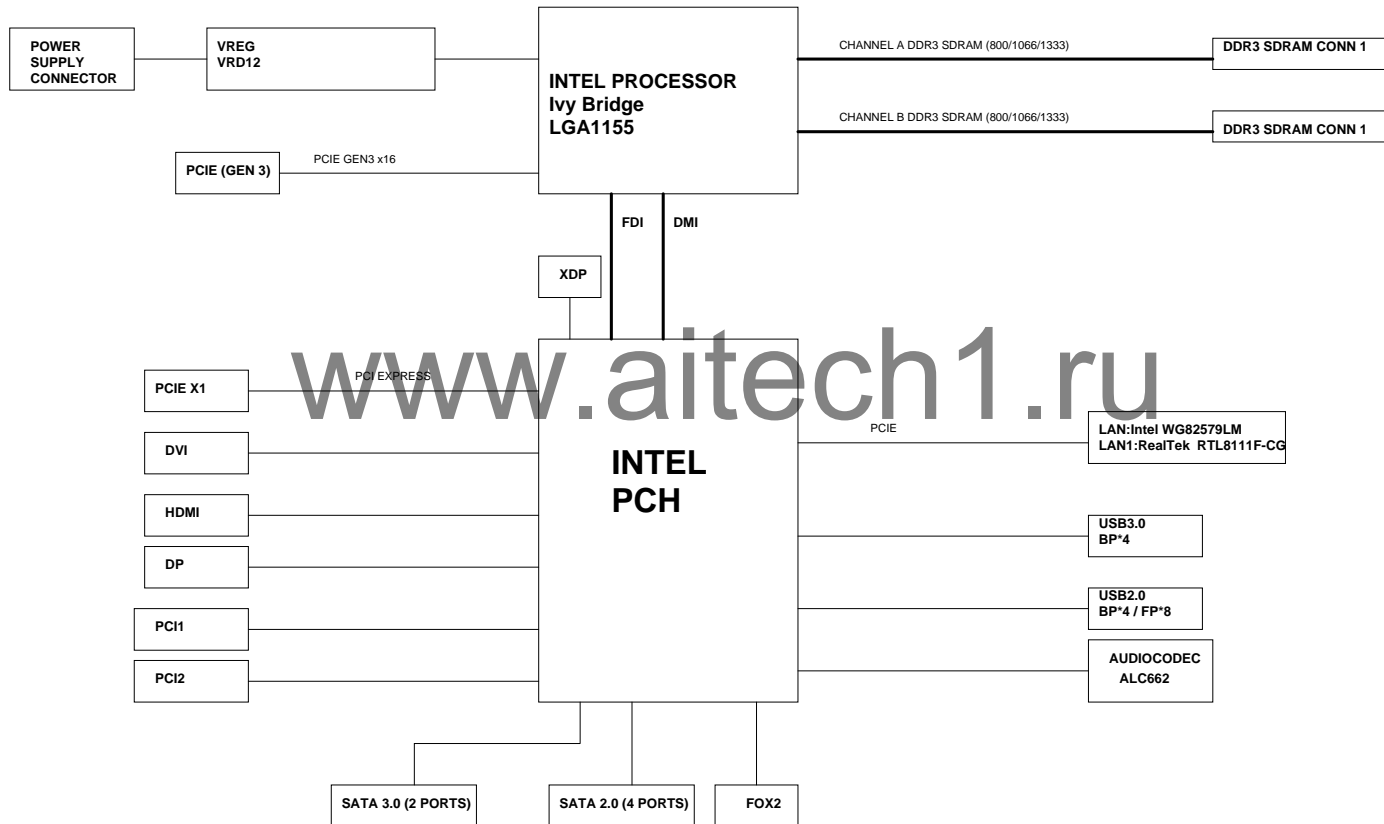
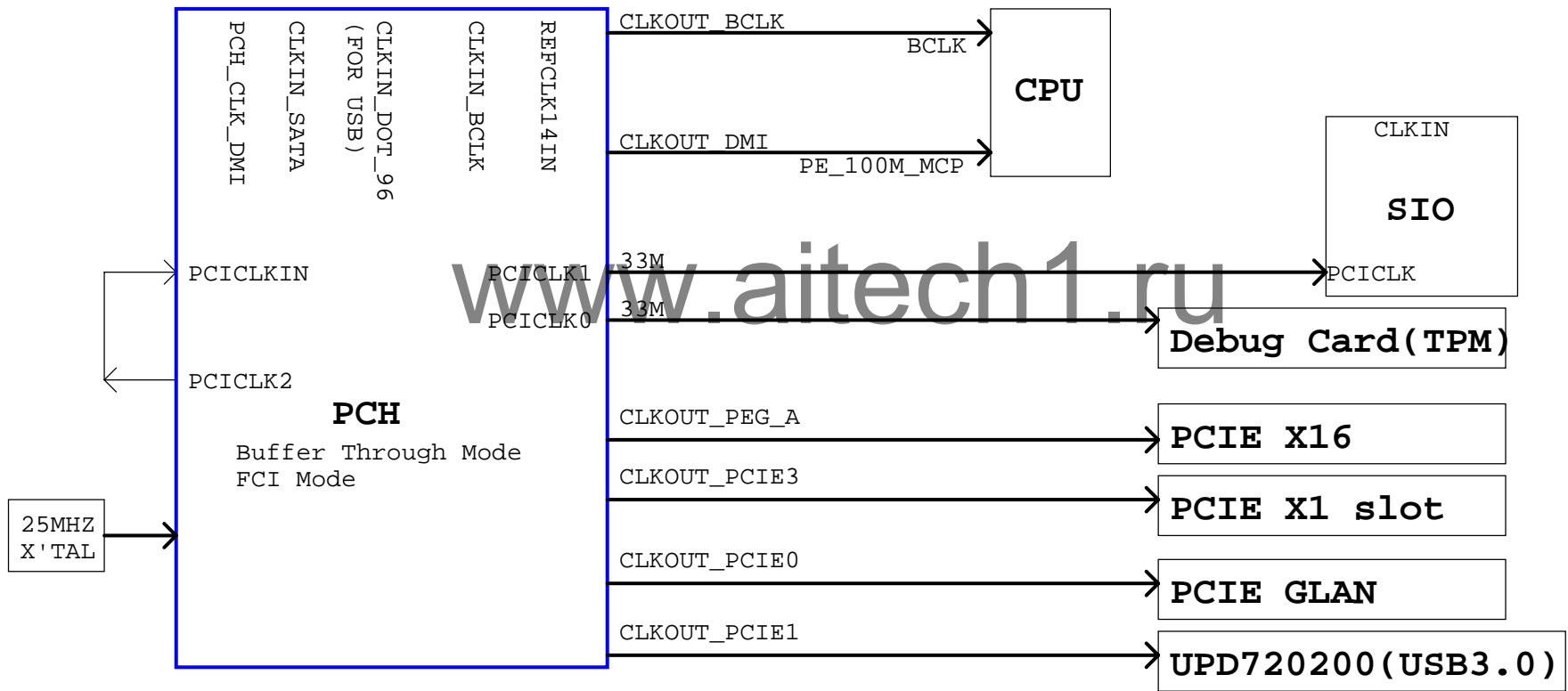


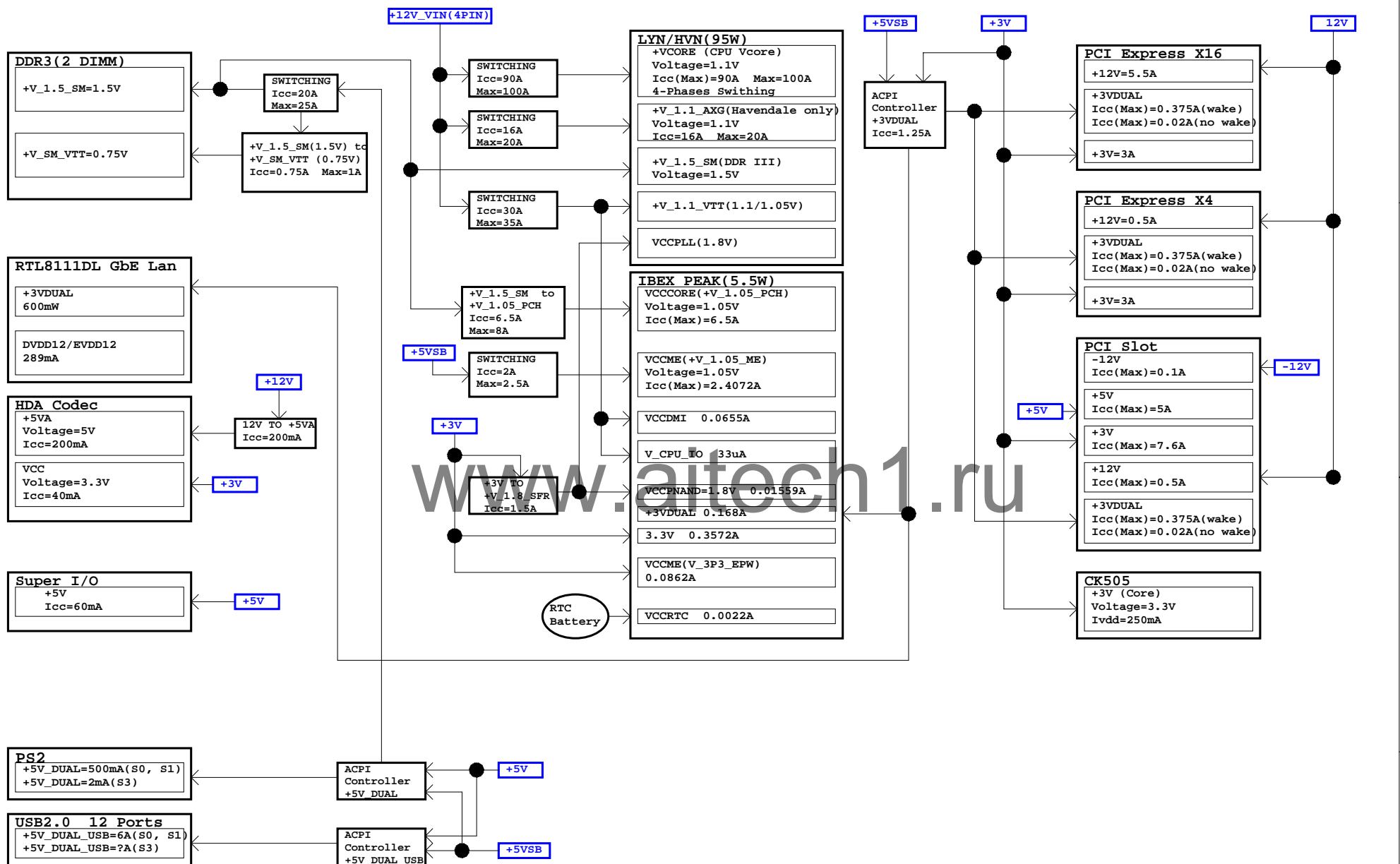
BLOCK DIAGRAM



CLOCK DISTRIBUTION



POWER DELIVERY MAP



POWER ON SEQUENCE

Figure 8-1. G3 w/RTC Loss to S4/S5 (With Deep S4/S5 Support) Timing Diagram

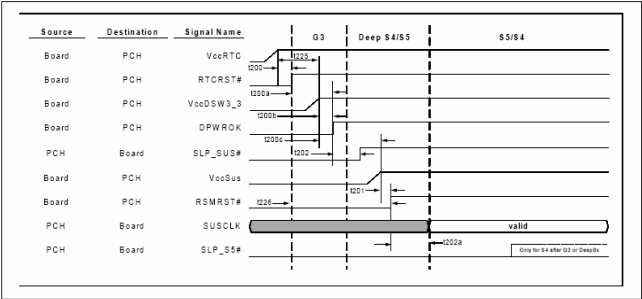


Figure 8-4. S3/M3 to S0 Timing Diagram

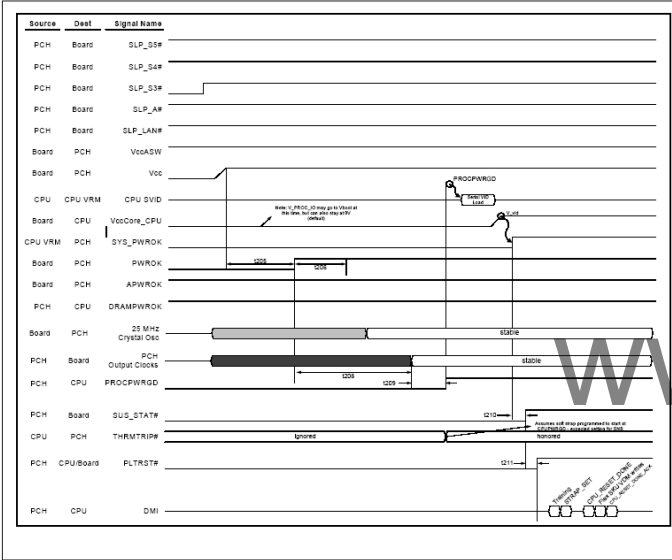


Figure 8-8. DRAMPWROK Timing Diagram

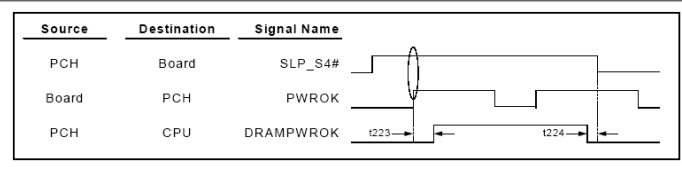


Figure 8-3. S5 to S0 Timing Diagram

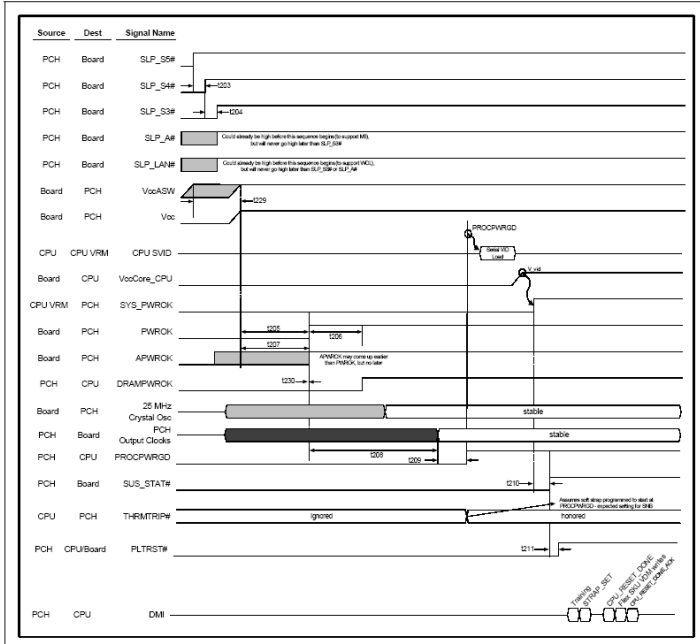
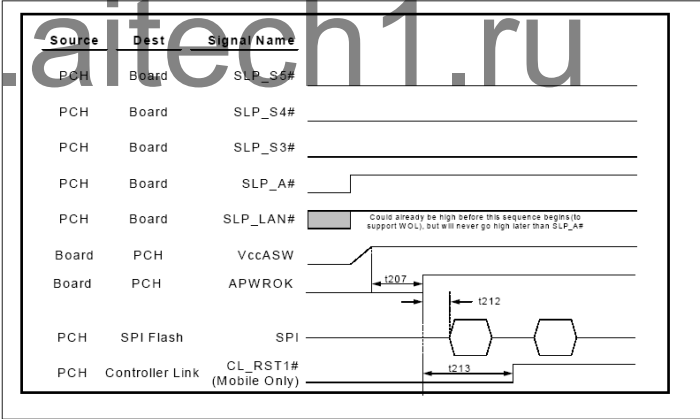
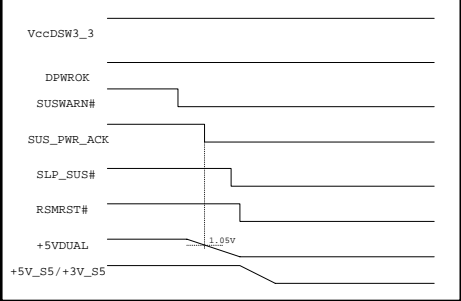


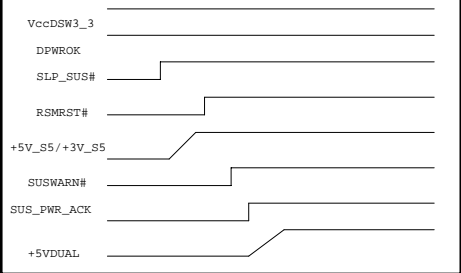
Figure 8-5. S5/Moff - S5/M3 Timing Diagram



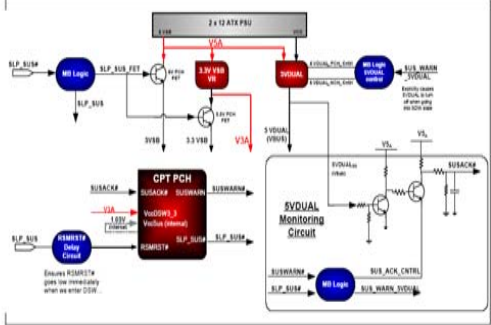
DSW Entry



DSW Exit



4-12. Example VBUS/VCCSUS Sequencing Circuitry using SUSWARN# & SUSACK#



Sequence Signal Name:

-

PCH_MEPWRGD

Power On Button

RESET BUTTON

Front Panel

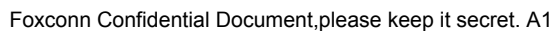
VRD 12

HD Audio

PCI Slot3

LAN

TPM/TCM



IRQ Routing Table

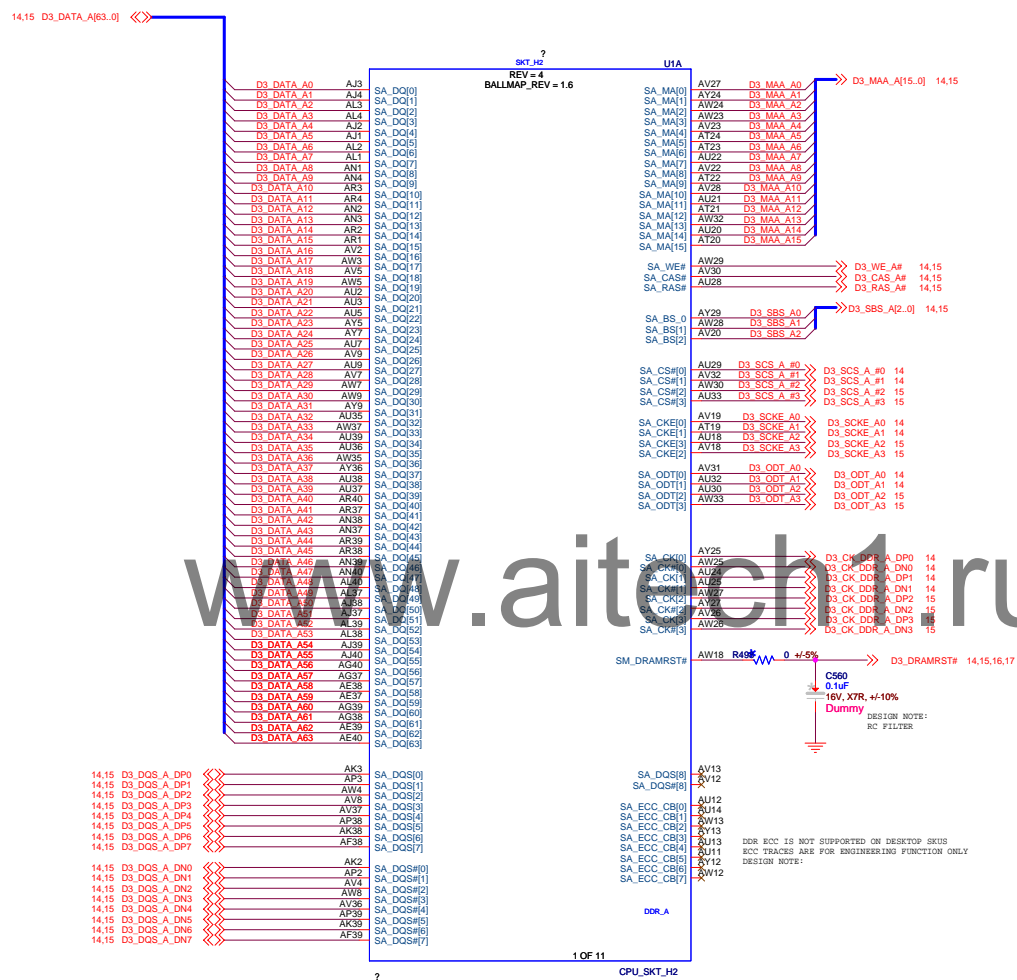
	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot1	A	B	C	D	17	0	0

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot2	B	C	D	A	19	2	2

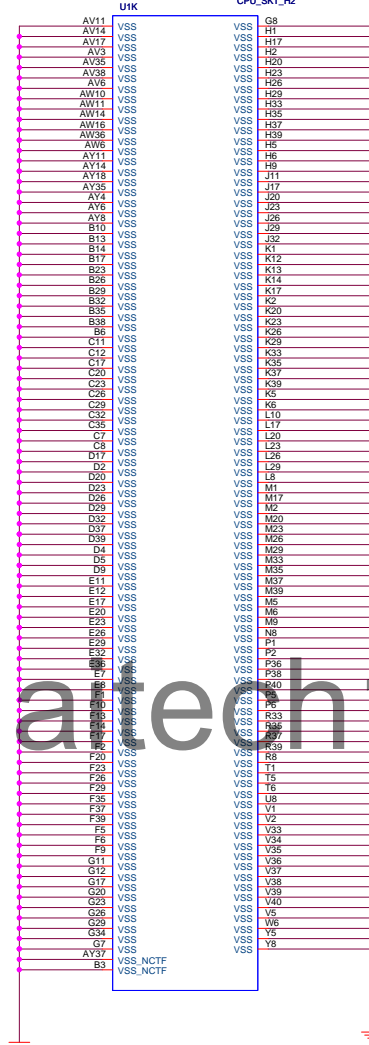
STRAPPING Table

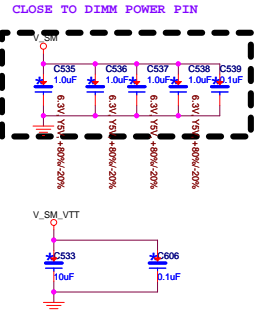
CPU side		
CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default
		0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express
		01: reserved
		10: 2x8 PCI Express
		11: 1x16 PCI Express Default

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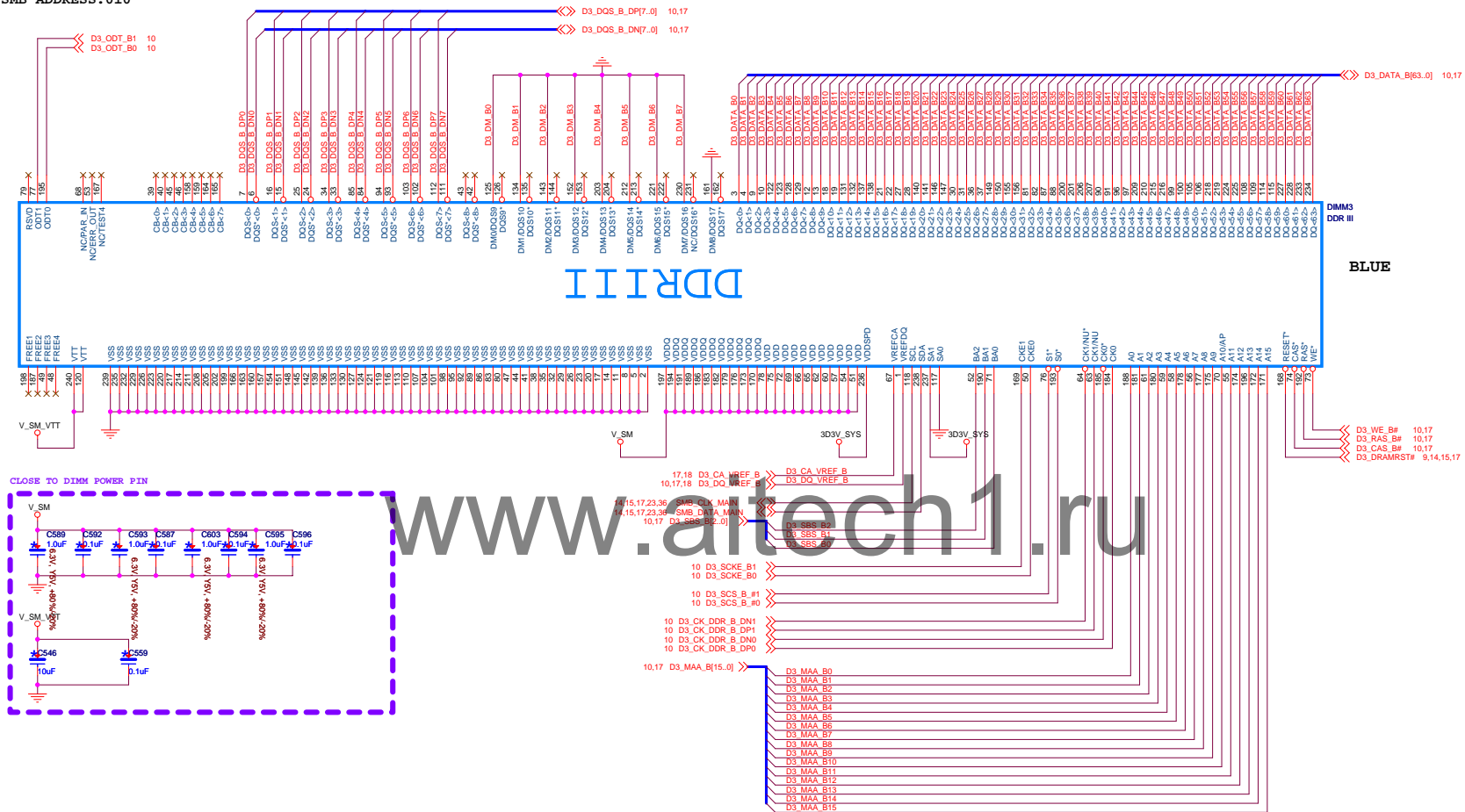


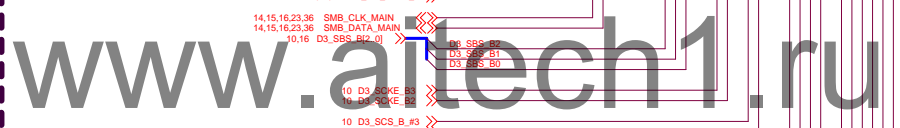
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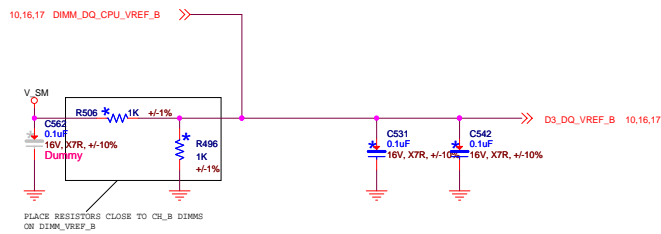
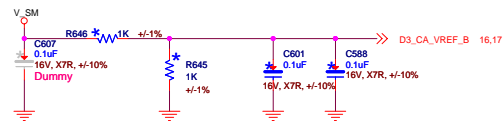
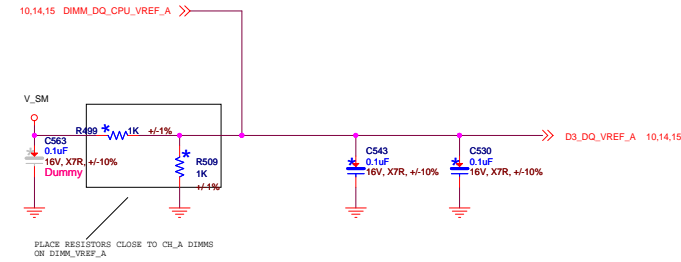
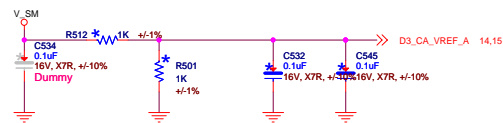


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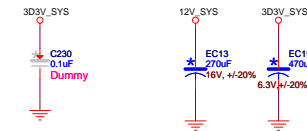
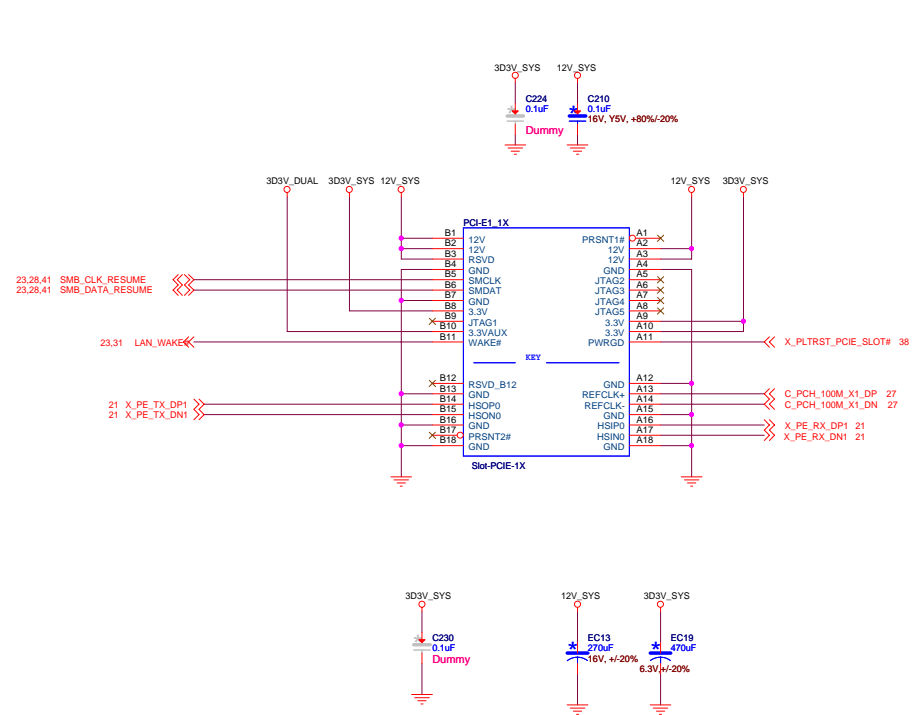
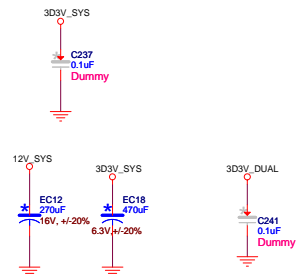
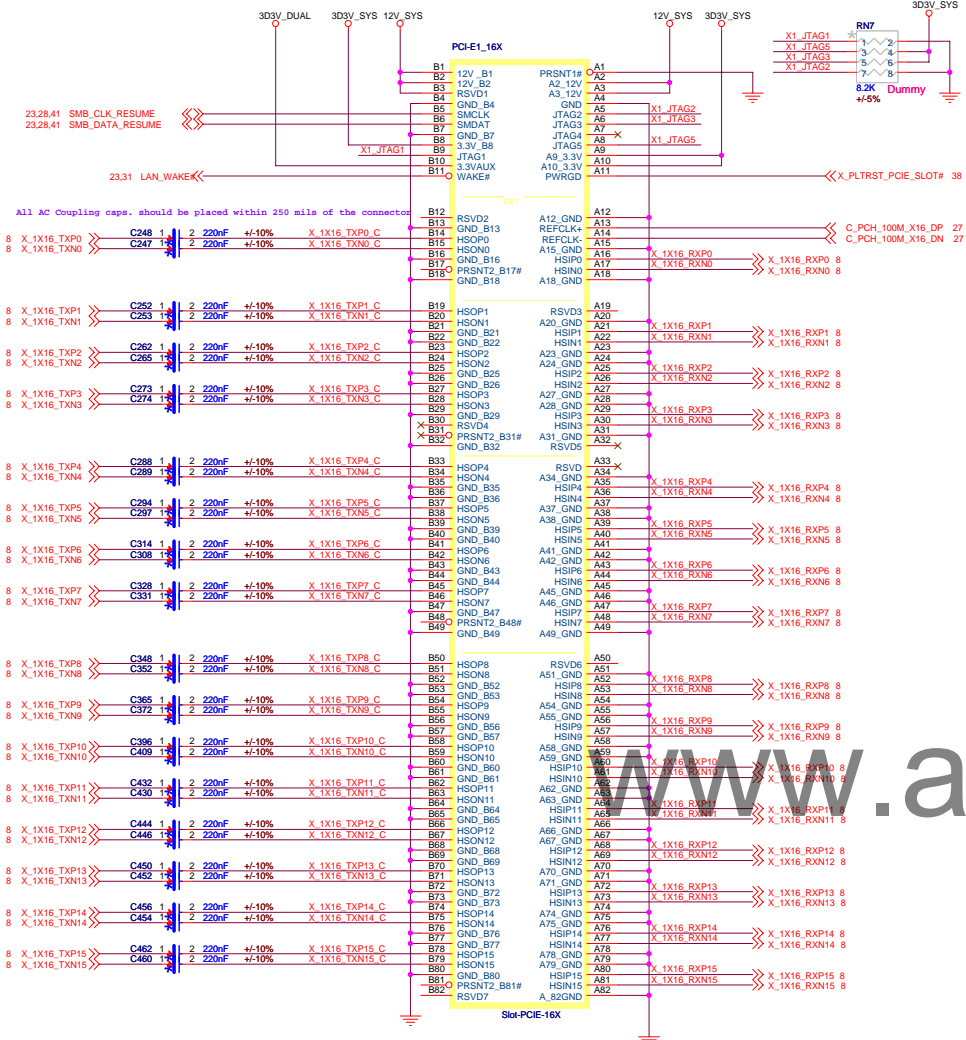
CHANNEL B DIMM 3
SMB ADDRESS:010



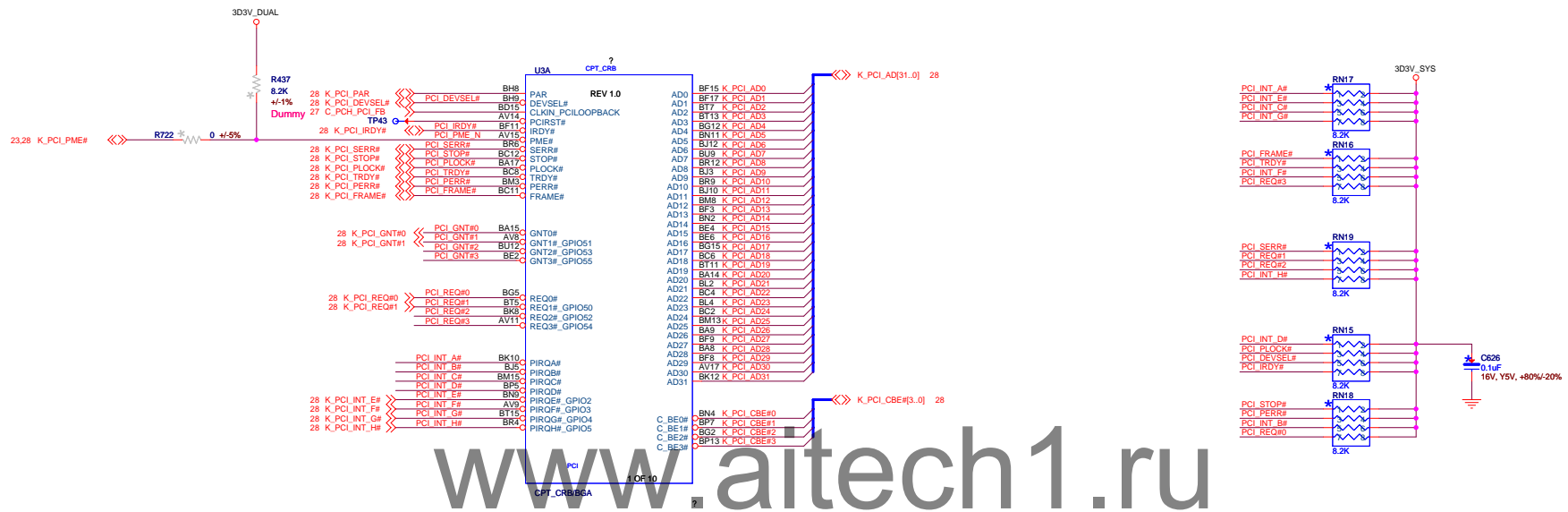




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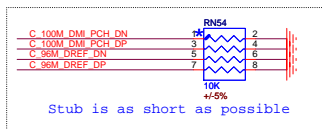
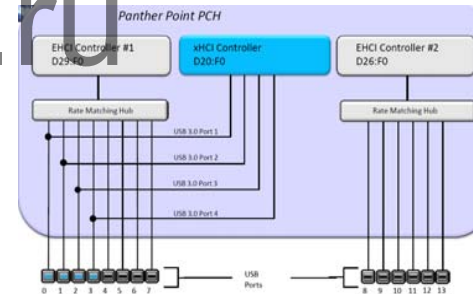
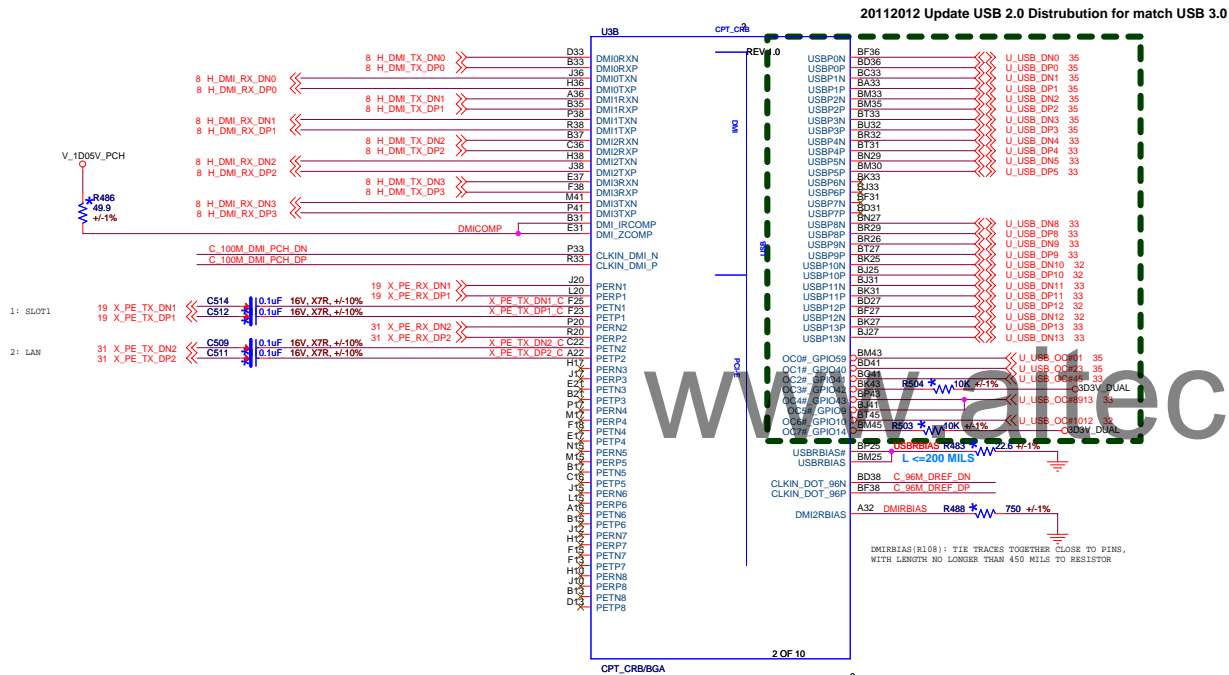
STRAP: Boot BIOSselect check whether GNT1 or SATA1GP(GPIO19)

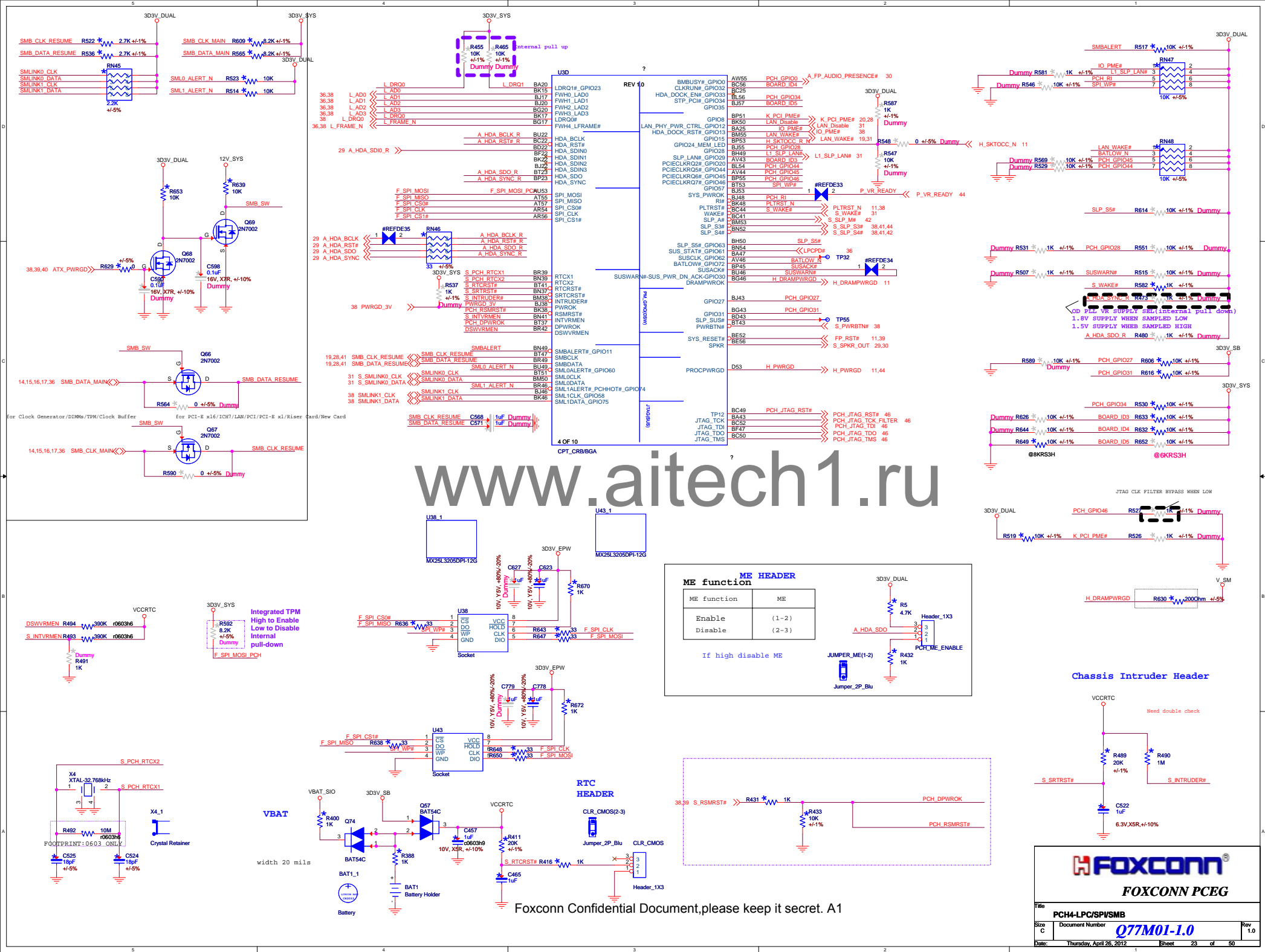
BOOT DEVICE	GNT1	SATA1GP
LPC	0	0
NAND	0	1
PCI	1	0
SPI	1	1



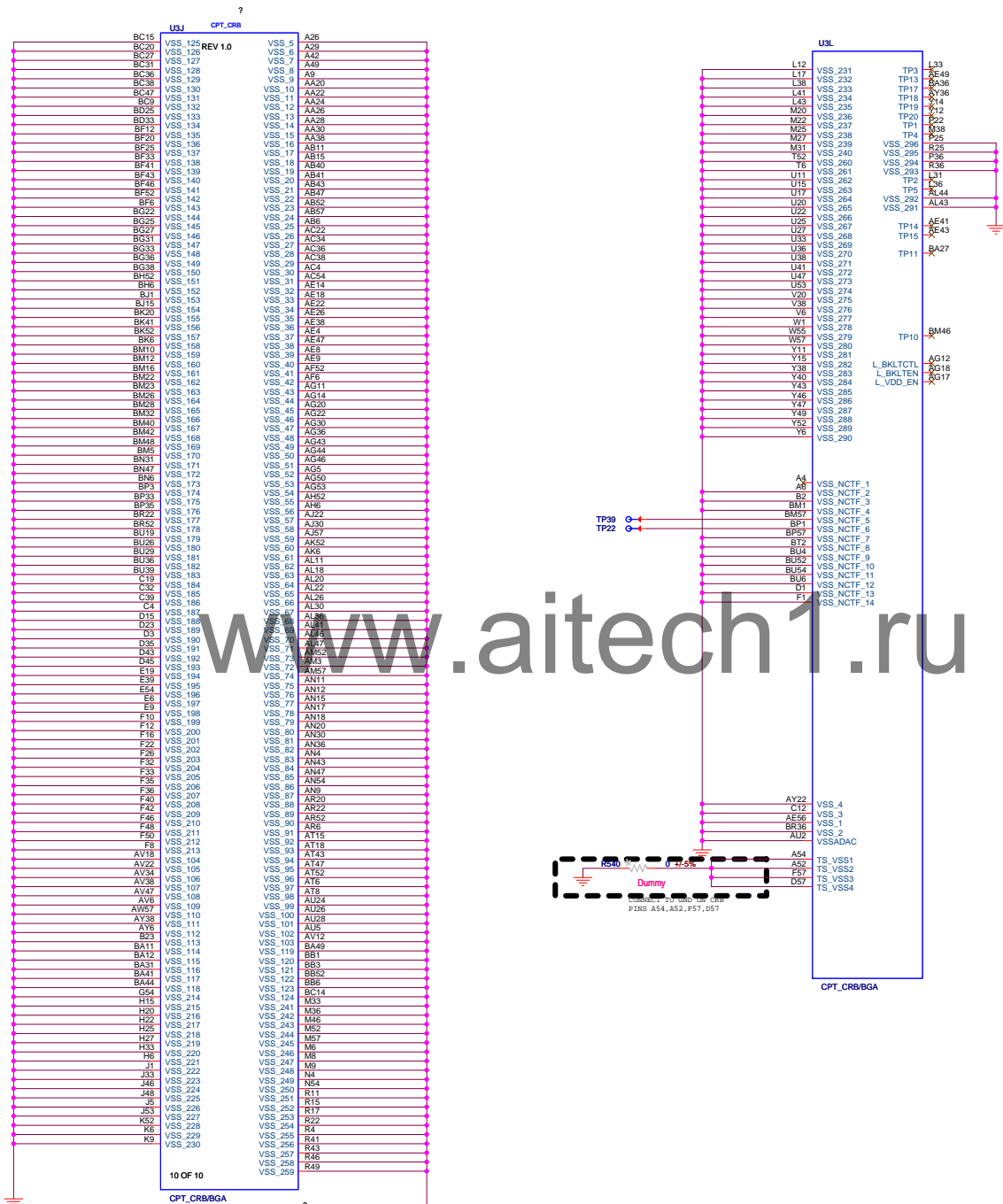
DG 0.7
GNT3 is top block swap mode:
connect to ground with 4.7k ohm weak
pull down resistor for top block swap mode
GNT2#/GPIO53:ESI strap for server platform
ONLY.Do not pull low.

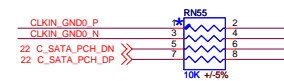
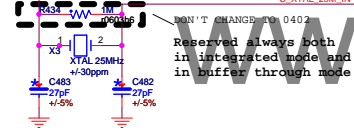
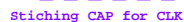












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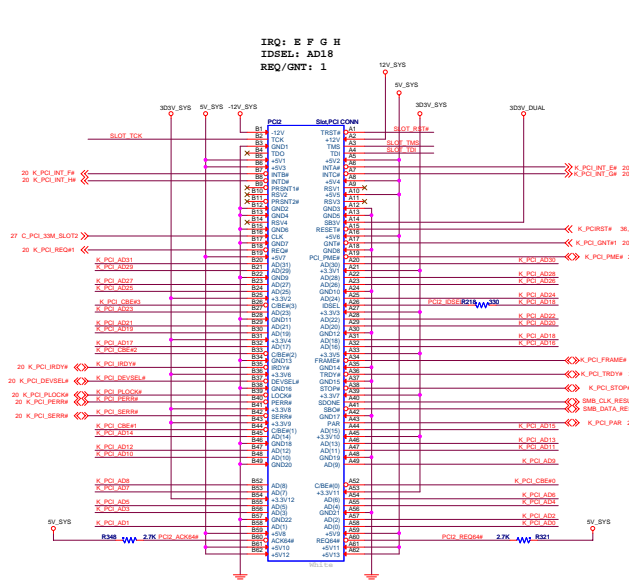
IRQ:  E F G H
IDSEL: AD18
REQ/GNT: 1

```

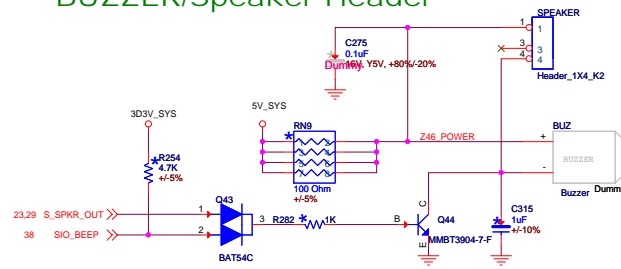
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IRQ:  E F G H
IDSEL: AD18
REQ/GNT: 1

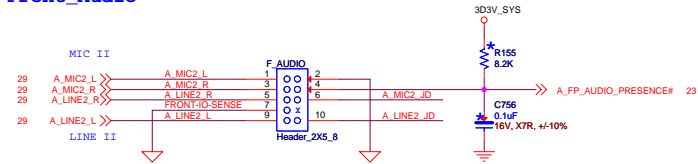
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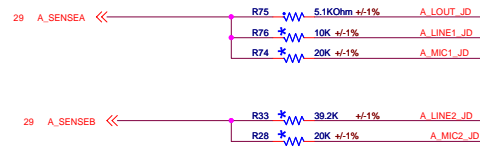
BUZZER/Speaker Header



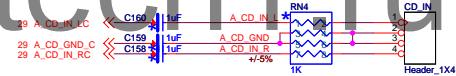
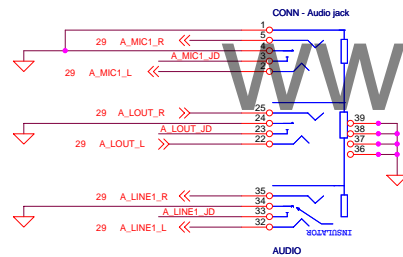
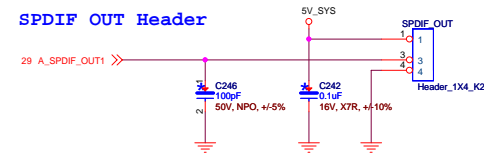
Front_Audio



JACK SENSE

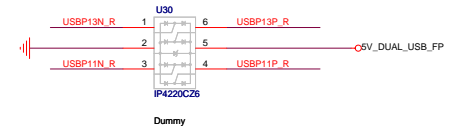
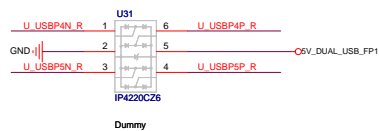
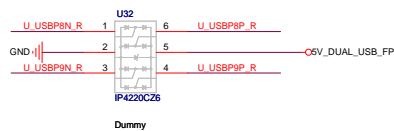
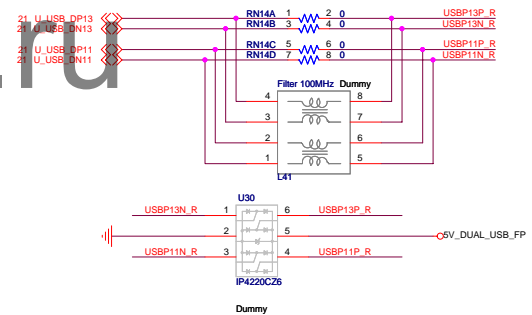
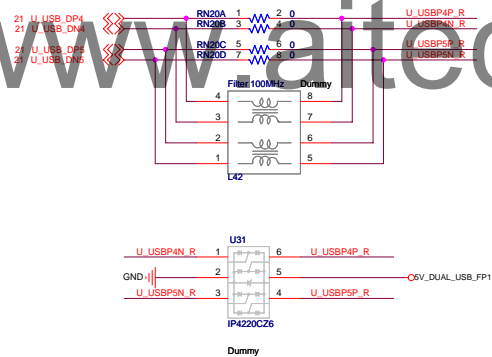
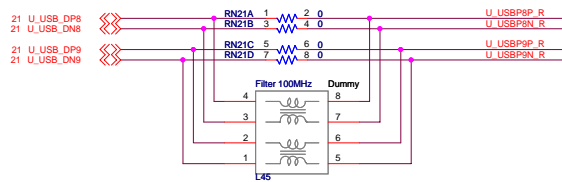
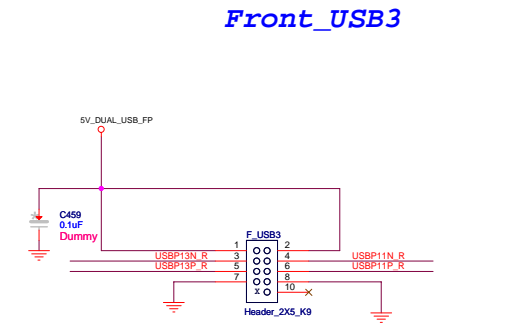
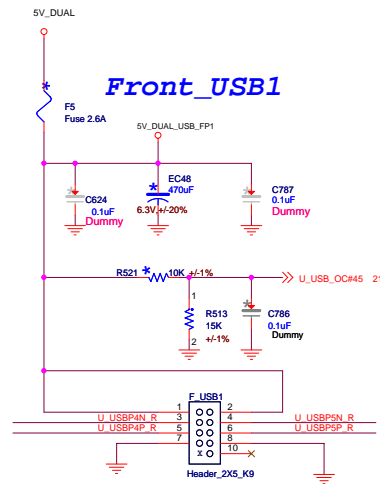
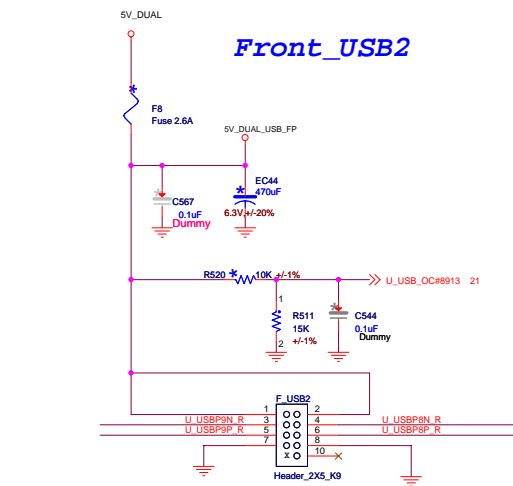


SPDIF OUT Header





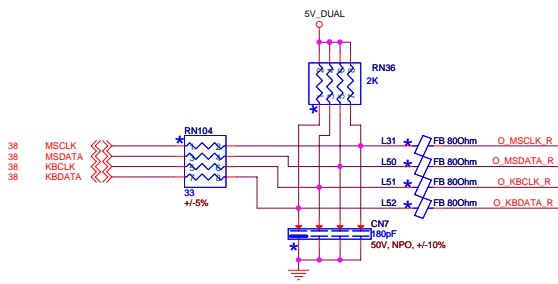
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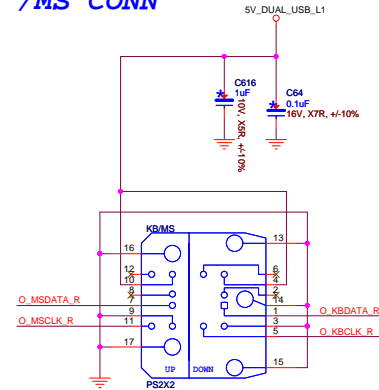
FOXCONN

FOXCONN PCEG

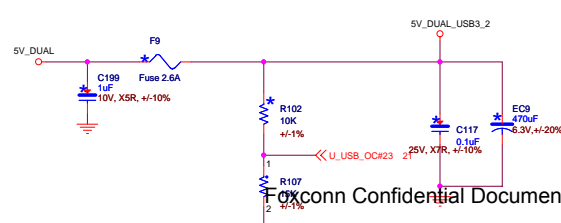
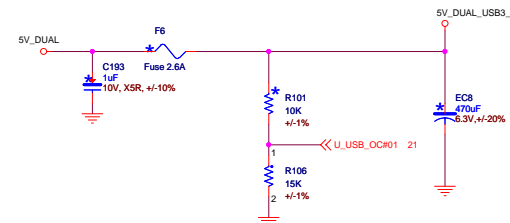
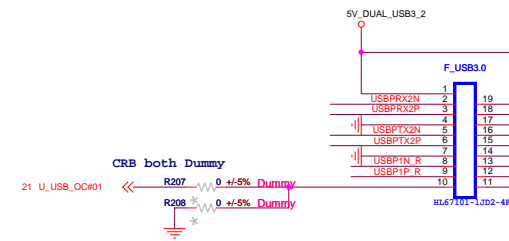
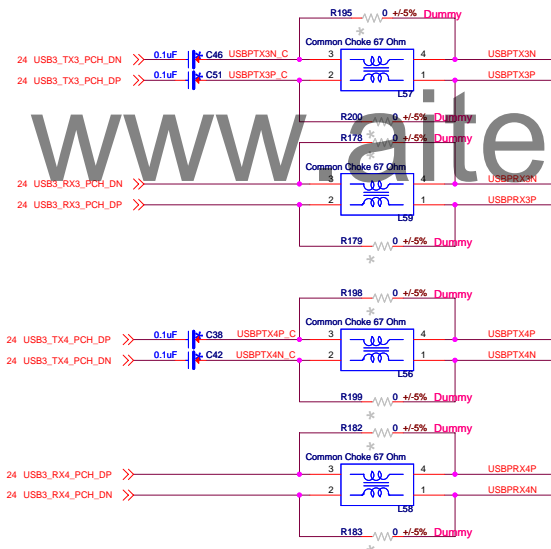
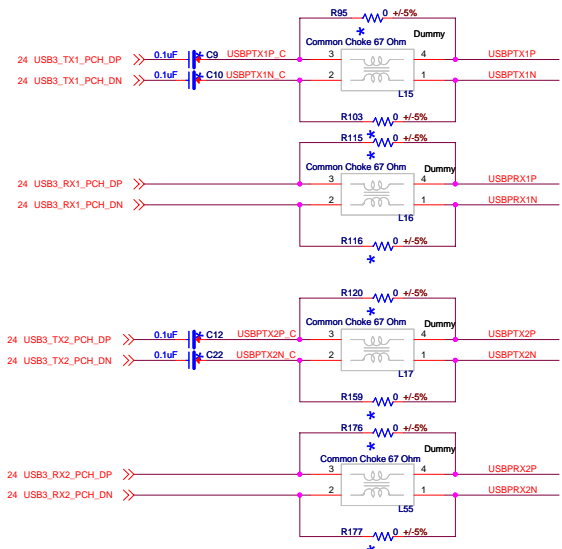
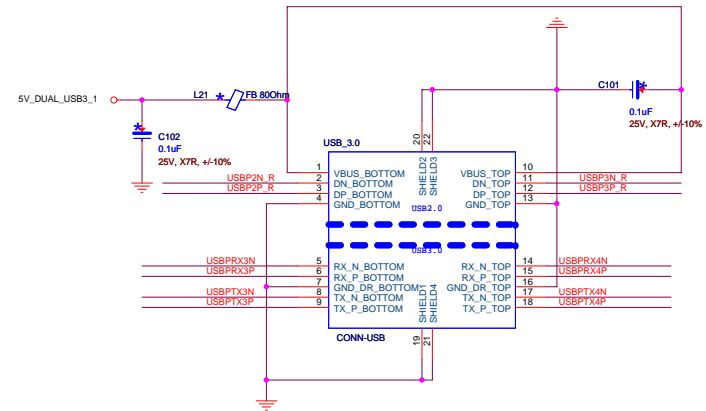
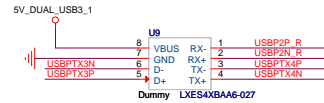
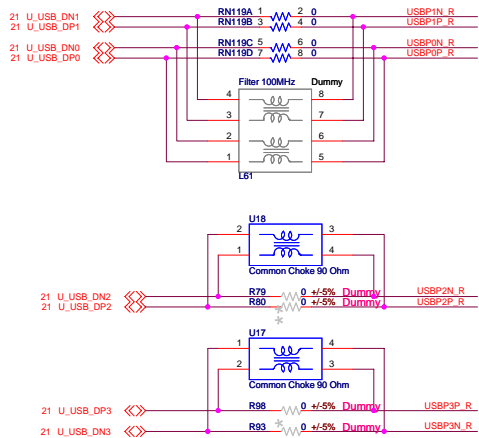
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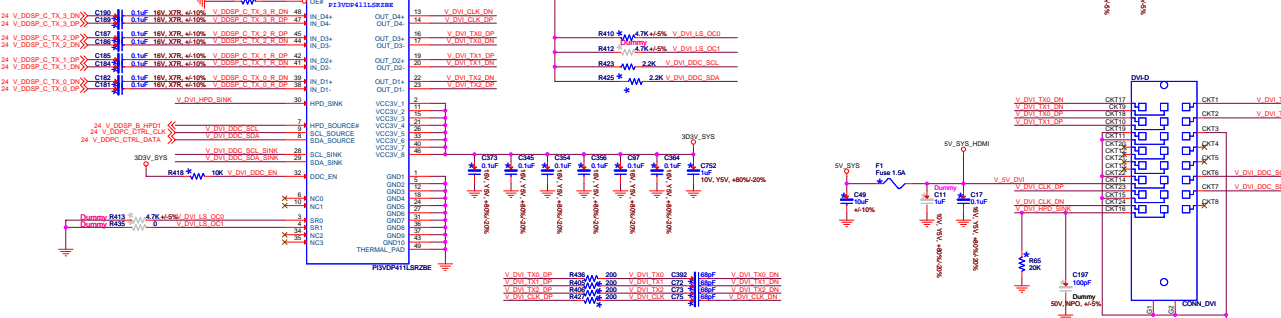


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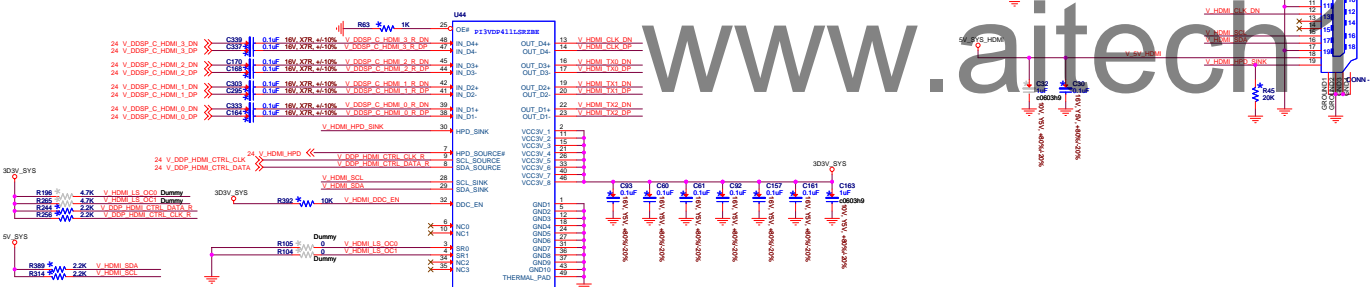


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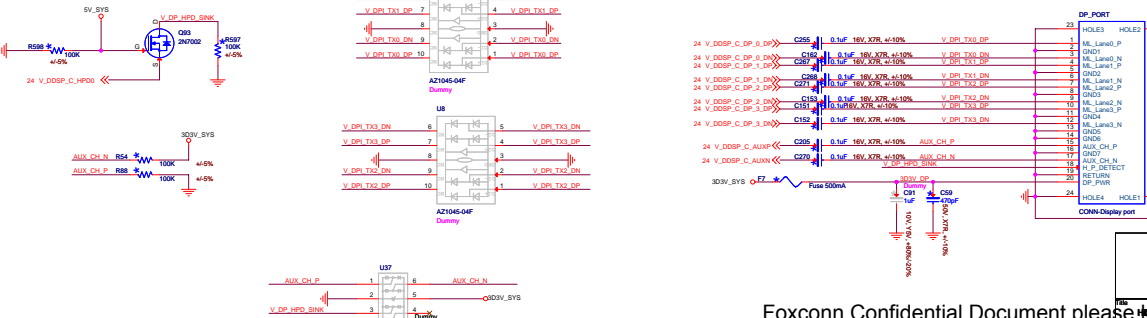
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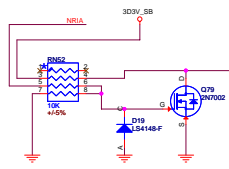
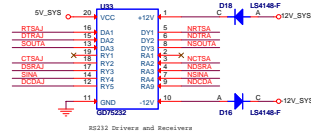
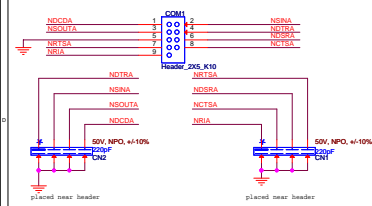
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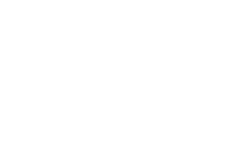
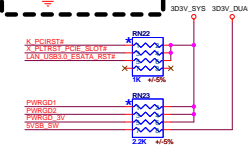
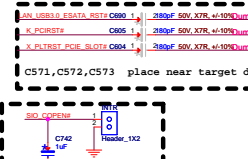
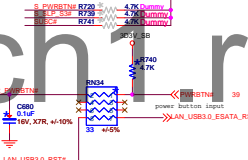
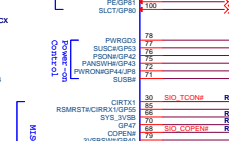
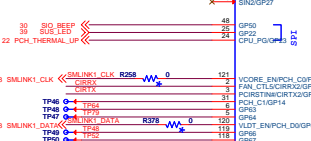
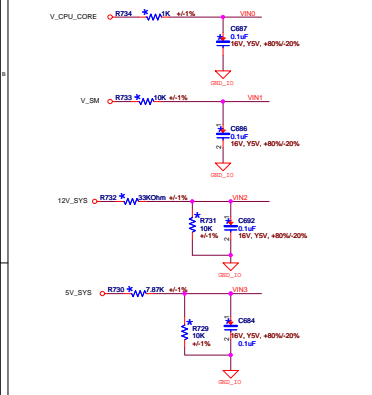
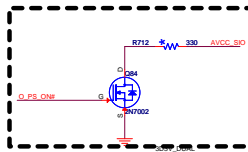
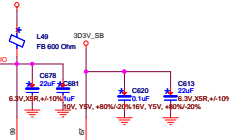
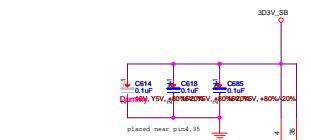
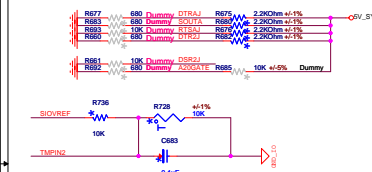
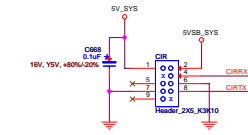
DP



COM HEADER



CIR



IT8728 Power On Strapping Options			
	Symbol	value	Description
JP4	KBPWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h(Fan half speed)
		10	The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
Pin 124 & 46		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 20h

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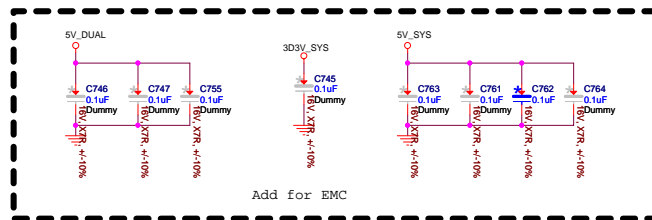
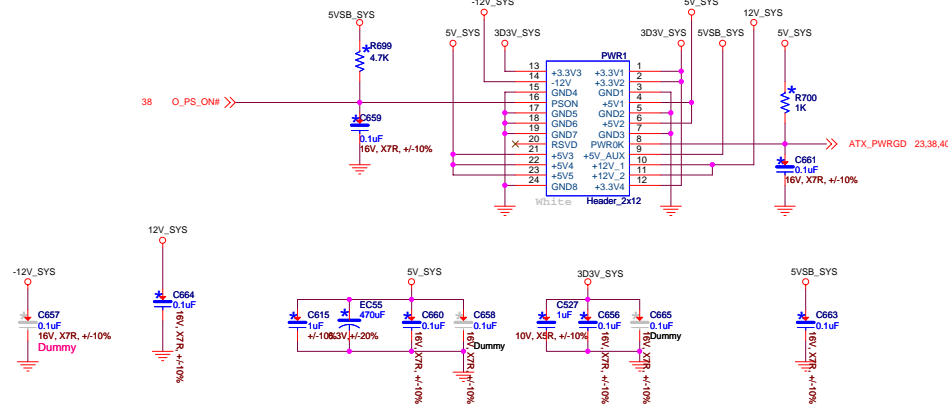
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Rev: 1.0

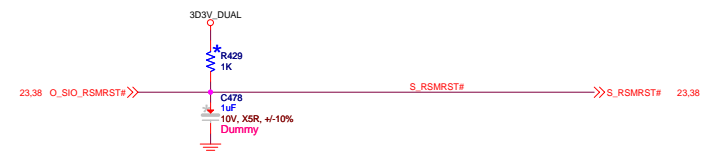
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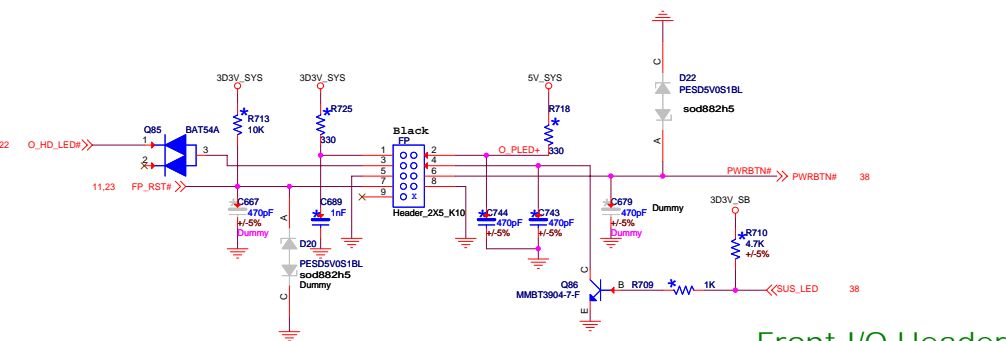
ATX POWER CONNECTOR



RESUME RESET LOGIC



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Front I/O Header

Front Panel Switch/LED			
HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Green)
GND	5	6	Power button
Reset button	7	8	Detect pin
Detect pin	9	10	Key

S0 : Power LED is on;
S1 : Power LED is blinking;
S3~S5: Power LED is off.

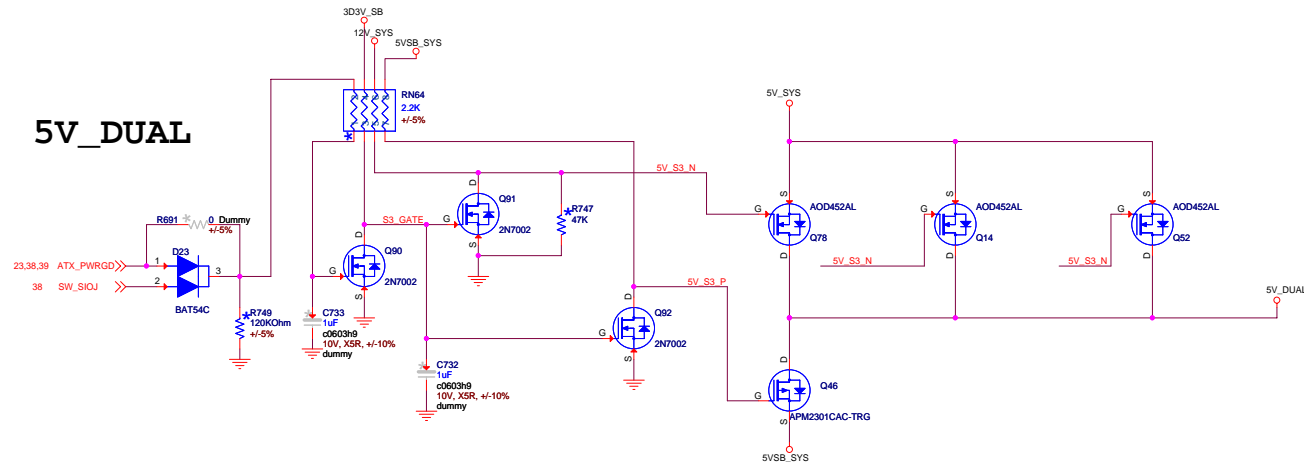
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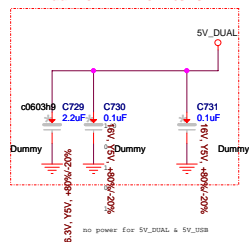
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5V_DUAL



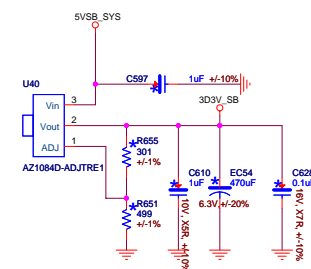
Add for EMI on 0929



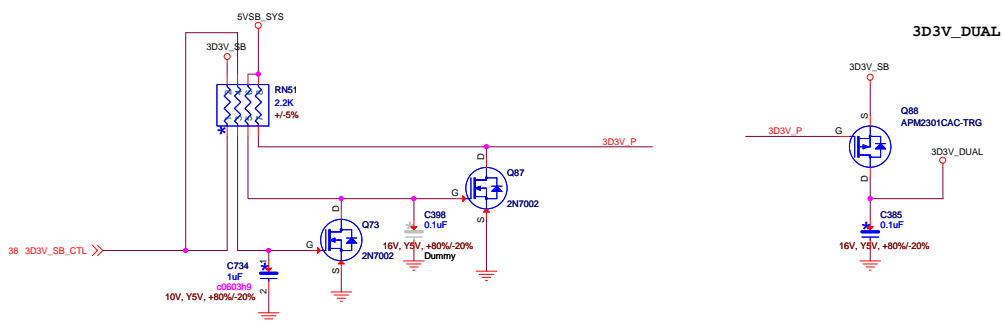
SW_SIOJ	ATX_PWRGD	5V_DUAL	5V_S3_N	5V_S3_P
S0	H	H	H	H
S1	H	L	L	H
S2	L	L	H	L

3D3V_SB

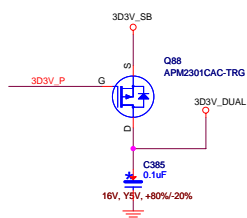
Max. output current = 3A



3D3V_DUAL

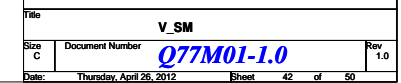
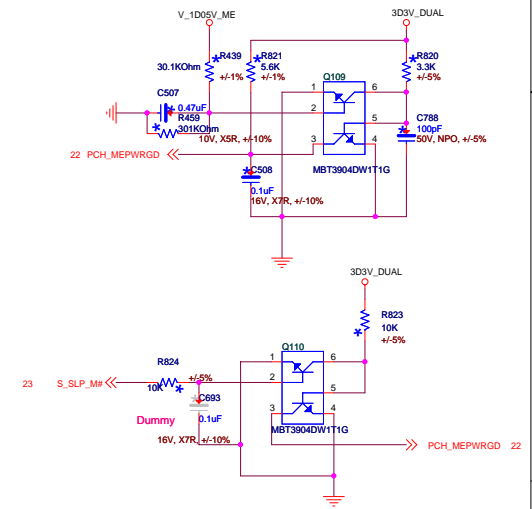
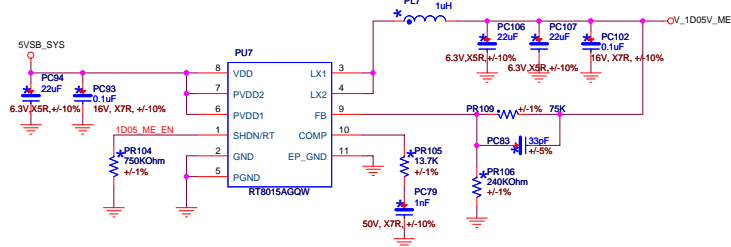
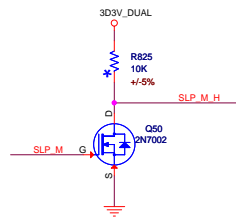
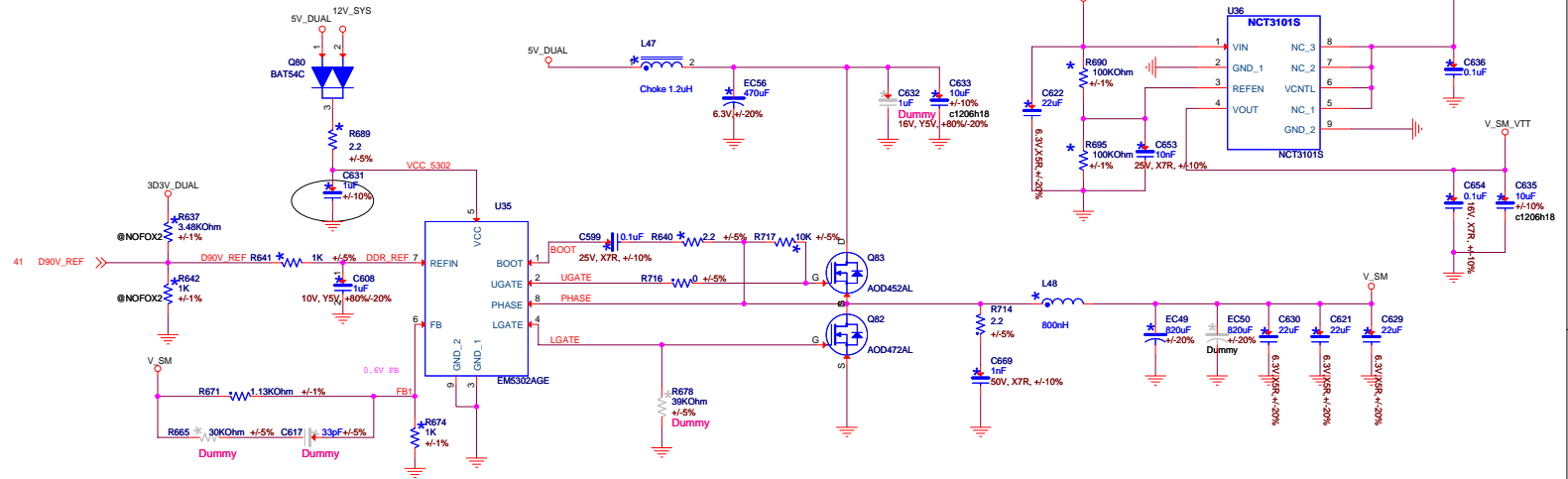


3D3V_DUAL

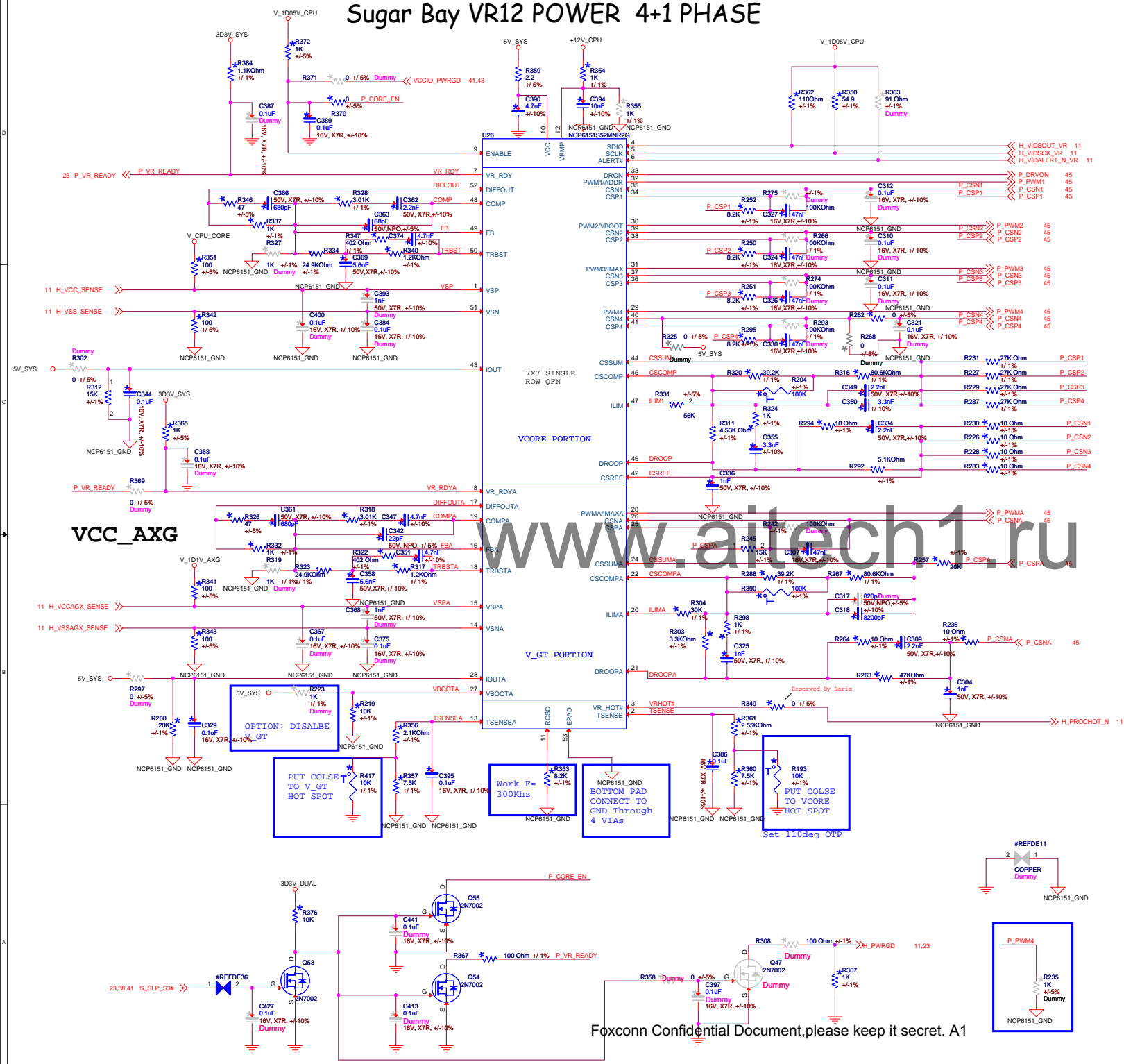


$V_{out} = V_{ref}(1 + R2/R1) + I_{adj}R2$
 $R1$ is Up Resistor.
 $I_{adj} = 50\mu A$
 $V_{ref} = 1.25V$

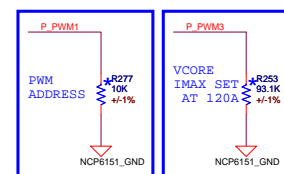
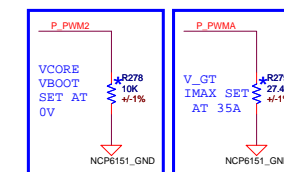
Max=40A
27A in design guide



Sugar Bay VR12 POWER 4+1 PHASE

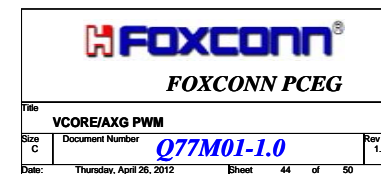


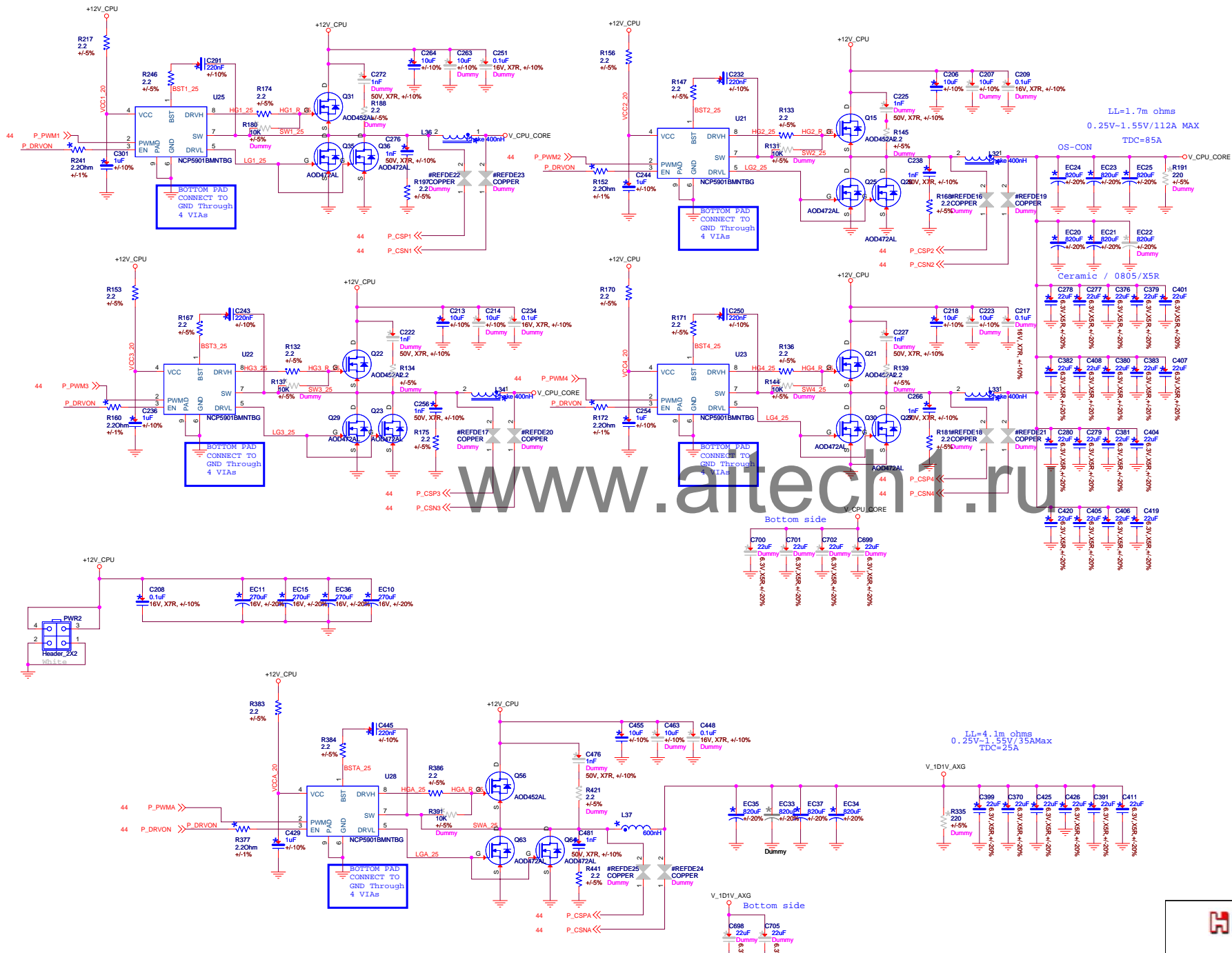
VCC_CORE



BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
125K	1.1V
165K	1.5V

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCOE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101





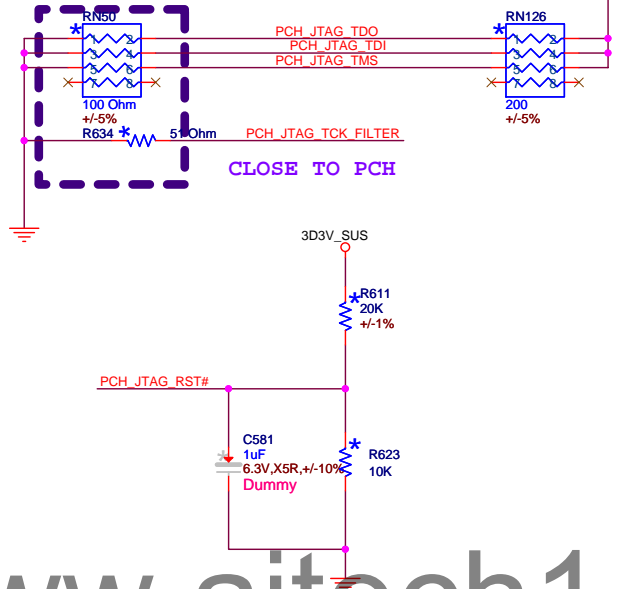
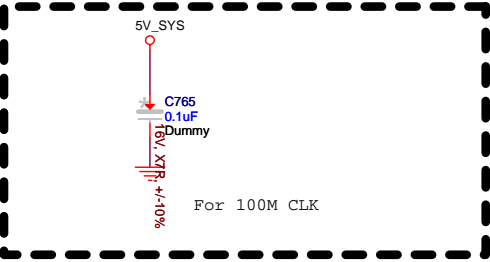
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File VCORE/AXG DRIVER		
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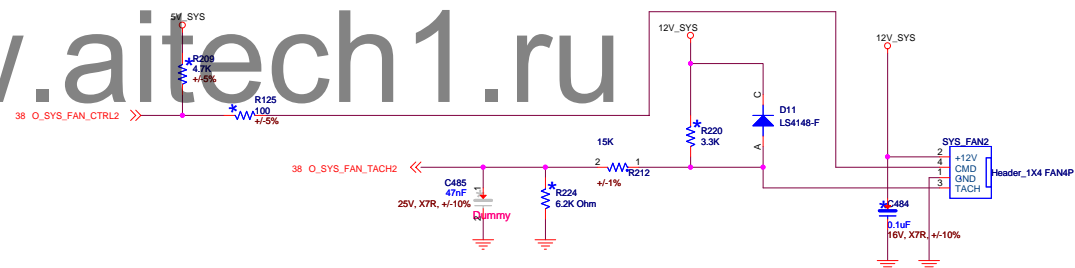
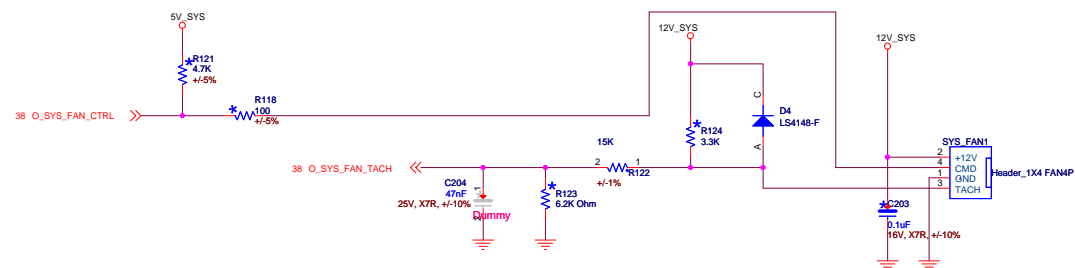
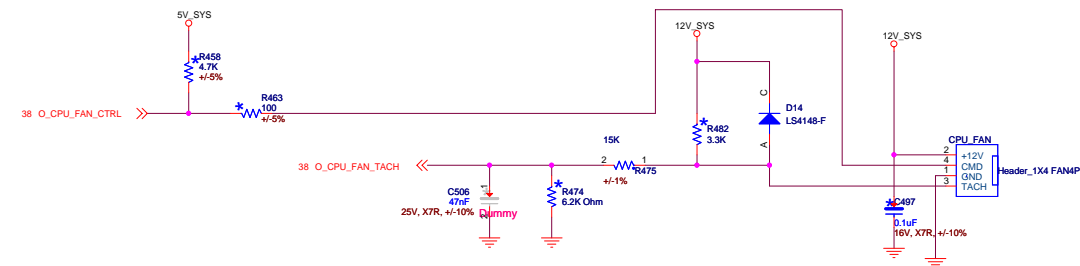
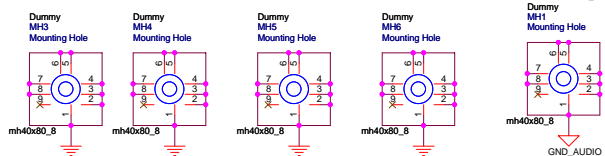
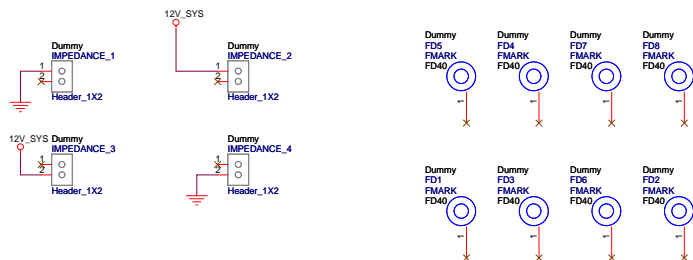
23 PCH_JTAG_TDO >> PCH_JTAG_TDO
 23 PCH_JTAG_TDI >> PCH_JTAG_TDI
 23 PCH_JTAG_TMS >> PCH_JTAG_TMS
 23 PCH_JTAG_TCK_FILTER >> PCH_JTAG_TCK_FILTER
 23 PCH_JTAG_RST# >> PCH_JTAG_RST#

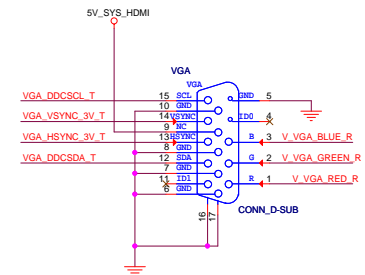
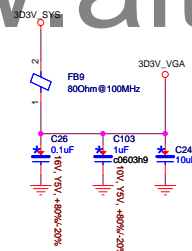
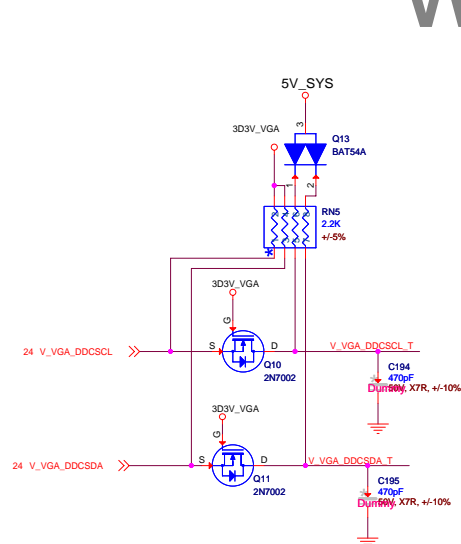
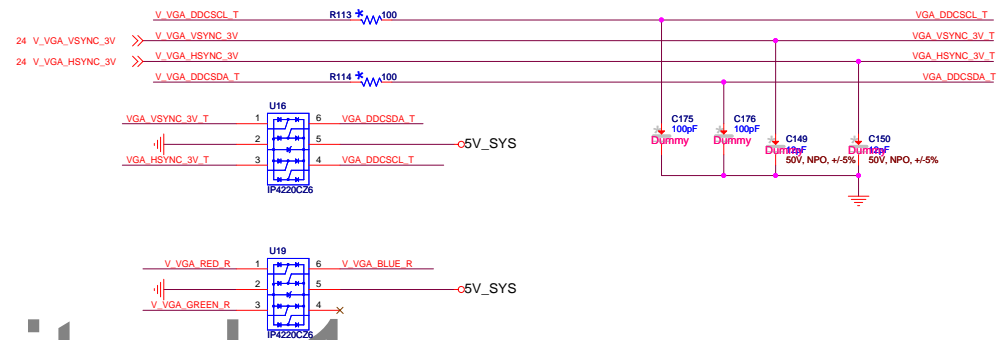


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Title		
Changelist		
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